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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,177	SUN, WEIN-TOWN	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-16 and 20-24* is/are allowed.

6)☒ Claim(s) *17 and 18* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 17-18 are rejected under 35 U.S.C. 102(e) as being anticipate by Choi et al. (US 2004/0056828 A1).

As to claim 17, Choi et al. teaches an electroluminescence device (paragraph 0002) comprising:

a plurality of scan lines (fig. 3, Gq-1,Gq);

a plurality of data lines (fig. 3, Dp,Dp+1); and

an array of pixels, each of the pixels being disposed near an intersection of one of the scan lines and one of the data lines (fig. 3) comprising:

a first circuit further comprising a first transistor, a second transistor and a capacitor, the capacitor including a first terminal coupled to a power supply, the first transistor including a gate electrode coupled to a second terminal of the capacitor, and the second transistor including a gate electrode receiving the voltage signal (fig. 3, items T3-T4, Cst, paragraph 0035);

a second circuit further comprising a third transistor and a fourth transistor, the third transistor including a gate electrode coupled to a gate electrode of the fourth

transistor (fig. 3, items T5,T2,paragraph 0041); and

a fifth transistor further comprising a gate electrode receiving the voltage signal, and an electrode receiving a current signal provided over a corresponding data line (fig. 3, item T1, paragraph 0035).

As to claim 18, Choi teaches the first circuit providing a voltage level across the capacitor in response to a first state of a voltage signal provided over a corresponding scan line, and maintaining the voltage level in response to a second state of the voltage signal signal (fig. 3, items T3-T4, Cst, paragraph 0035).

Response to Arguments

2. Applicant's arguments filed 06/10/07 have been fully considered but they are not persuasive:

On page 18, 3rd paragraph of Remark, Applicant's stated that in the application, however, the voltage signal received by the gate of the second transistor is the same as the signal received by the gate of the fifth transistor. Comparing with Choi (reference to FIG. 3), the gate of item T1 does not connect to the gate of item T4 such that the signal received by gate of item T1 is different from the signal received by gate of item T4. However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the voltage signal received by the gate of the second transistor is the same as the signal received by the gate of the fifth transistor) are not recited in the rejected claim(s).

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Allowable Subject Matter

3. Claims 1-16, 20-24 are allowed.

Relative to independent claim 1 the major difference between the teaching of the prior art of record (Choi) and the instant invention is that a first circuit further comprising a first transistor, a second transistor and a capacitor, the capacitor including a first terminal coupled to a power supply, the first transistor including a gate electrode coupled to a second terminal of the capacitor, and the second transistor including a gate electrode receiving the voltage signal, wherein the first circuit provides a voltage level across the capacitor in response to the first state of the voltage signal, and maintains the voltage level in response to the second state of the voltage signal; and
a second circuit further comprising a third transistor and a fourth transistor, the third transistor including a gate electrode coupled to a gate electrode of the fourth transistor.

Claims 2-10 depend on claim 1.

Relative to independent claim 11 the major difference between the teaching of the prior art of record (Choi) and the instant invention is that a first circuit further comprising a first transistor, a second transistor and a capacitor providing a voltage level across the capacitor in response to the first state of the voltage signal, and maintaining the voltage level in response to the second state of the voltage signal; and

a second circuit further comprising a third transistor and a fourth transistor, the third transistor including a channel width/length value N times a channel width/length value of the fourth transistor; wherein the first circuit provides a current of (1 + I/N) I during the first and second states of the voltage signal, and the second circuit provides a current of 1IN I in response to the first state of the voltage signal.

Claims 12-16 depend on claim 11.

Relative to independent claim 20 the major difference between the teaching of the prior art of record (Choi) and the instant invention is that providing a voltage level across the capacitor in response to the first state of the voltage signal provided over a corresponding scan line; maintaining the voltage level in response to the second state of the voltage signal; fourth electrode of the fourth transistor; providing a first current of (1 + I/N) I providing each of the pixels with a second circuit including a third transistor and a transistor, the third transistor including a gate electrode coupled to a gate from the first circuit during the first and second states of the voltage signal; and providing a second current of (I/N) I from the second circuit in response to the first state of the voltage signal, N being the ratio of a channel width/length of the third transistor to that of the fourth transistor.

Claims 21-26 depend on claim 20.

4. Claims 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 19 the major difference between the teaching of the prior art of record (Choi) and the instant invention is the current signal has a magnitude I, the first circuit providing a first current of (1 + I/N) I during the first and second states of the voltage signal, and the second circuit providing a second current of (I/N) I in response to the first state of the voltage signal, N being the ratio of a channel width/length of the third transistor to that of the fourth transistor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
08.14.07

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